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Class Subclass  
ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE	
EA SCANNED	9/14/01	Q.A. AG

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/768911		40 253	37.2	2011	ZARNEKE 2827

APPLICANTS

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TITLE

Integrated circuit product having reverse engineering and method for fabricating the same using vias without metal terminations

PTO-2040  
12/89

ASSURING CLASSIFICATION

		DRAWINGS			
		Sheet Drawing	Box Drawing	Print File	Total Sheets
				2	2
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.		<b>NOTICE OF ALLOWANCE MAILED</b> <i>David A. Zaluck 12/1/01</i> (Assistant Examiner) (Date)			
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____.		<b>ALBERT W. PALADINI</b> <b>PRIMARY EXAMINER</b> <i>Albert W. Paladini 12-13-01</i> (Primary Examiner) (Date)			
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.		<b>ISSUE FEE</b> (Legal Instruments Examiner) (Date) <b>Amount Due</b> <i>\$1,580.00</i> <b>Date Paid</b> <i>12/13/01</i>			
<b>ISSUE BATCH NUMBER</b> <i>J. M. Chaviller 12/16/01</i> (Date)					

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(FACE)

DRAWINGS IN FILE

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